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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (original) A voltage down converter comprising:

an input node receiving an external voltage VEXT;

a driver unit selectively coupling the input node to an internal voltage supply node in response to a drive control signal;

a reference voltage generator providing a voltage VREF;

a hysteresis timing unit responsive to a first control signal and generating one or more control signals selected from the group consisting of a second control signal VHYST- and a third control signal VHYST+; and

a comparator unit coupled to the internal voltage supply node, VREF, VHYST- and VHYST+ and coupled to the driver unit to generate the drive control signal, the comparator unit shifting a trip point of the comparator in response to the second and third control signals.

2. (original) The voltage down converter of claim 1 wherein the comparator unit further comprises:

a differential input stage having a first input coupled to a signal that is proportional to the voltage on the internal voltage supply node, a second input coupled to VHYST-, a third input coupled to VREF, and a fourth input coupled to VHYST+, and an output, wherein the input stage generates the drive control signal.

3. (original) The voltage down converter of claim 2 wherein the differential input stage comprises:

a first branch within the differential input stage comprising a first load device, a primary current path providing a current through the first load device that is proportional to the voltage on the internal voltage supply node, and supplementary current path providing a current through the first load device when the VHYST- signal is active; and

a second branch within the differential input stage comprising a second load device, a primary current path providing a current through the second load device that is responsive to the reference voltage, and supplementary current path providing a current through the second load device when the VHYST+ signal is active.

4. (original) The voltage down converter of claim 3 wherein the primary current path of the first branch comprises a first field effect transistor coupled in series with the first load device having a gate electrode coupled to a signal that is proportional to the voltage on the internal voltage supply node; and

wherein the supplementary current path of the first branch comprises a second and a third field effect transistor coupled in series with each other and with the first load device, wherein the gate of the second field effect transistor is coupled to the VHYST- signal and the gate of the third field effect transistor is coupled to the reference voltage generator.

5. (original) The voltage down converter of claim 3 wherein the primary current path of the second branch comprises a first field effect transistor coupled in series with the second load device having a gate electrode coupled to the reference voltage generator; and

wherein the supplementary branch of the second current path comprises a second and a third field effect transistor coupled in series with each other and with the second load device, wherein the gate of the second field effect transistor

is coupled to the VHYST+ signal and the gate of the third field effect transistor is coupled to the reference voltage generator.

6. (original) The voltage down converter of claim 1 wherein the hysteresis timing unit further comprises:

a first input coupled to the drive control signal;

a second input coupled to receive a clock signal, wherein the clock signal is selected to anticipate activation and deactivation of a high current load coupled to the internal voltage supply node; and

a logic circuit for combining signals on the first and second inputs to generate the first control signal VHYST-.

7. (original) The voltage down converter of claim 6 wherein the hysteresis timing unit further comprises:

a voltage shift circuit coupled to the second input to shift the signal on the second input from a logic level based on the internal supply voltage to a logic level compatible with the external voltage.

8. (original) A method for converting voltage VCC supplied to a pin of an integrated circuit to a lower internal voltage VCCI on an internal voltage supply node, the method comprising the steps of:

generating a first signal proportional to the internal voltage;

coupling the first signal to a comparator, the comparator operating to generate a second signal indicating when the first signal is above or below the trip point;

monitoring a clock signal to anticipate current load in the integrated circuit; and

shifting the trip point in response to the clock signal.

9. (new) The method of claim 8, further comprising the step of:

programming the trip point by adjusting a size of one or more transistors used to implement the comparator.

10. (new) The method of claim 8, further comprising the step of:

programming the trip point by programatically coupling a plurality of transistors used to implement the comparator in parallel using field programmable techniques.

11. (new) The method of claim 8, further comprising the step of:

programming the trip point by programatically coupling a plurality of transistors used to implement the comparator in parallel using mask programmable techniques.

12. (new) The method of claim 8, further comprising the step of:

programming a hysteresis voltage by adjusting a size of one or more transistors used to implement the comparator.

13. (new) The method of claim 8, further comprising the step of:

generating a first hysteresis control signal and a second hystersis control signal from the clock signal, the first hysteresis control signal being active when the trip point is to be shifted to a higher voltage, and the second hysteresis control signal being active when the trip point is to be shifted to a lower voltage.

14. (new) The method of claim 8, further comprising the step of:

using the clock signal to anticipate a voltage droop condition; and

shifting the trip point higher when the voltage droop condition is anticipated.

15. (new) The method of claim 8, further comprising the step of:

using the clock signal to anticipate a voltage overshoot condition; and

shifting the trip point lower when the voltage droop condition is anticipated.

16. (new) The voltage down converter of claim 1, wherein the trip point is initially set at a level determined by sizes of transistors in the comparator unit.

17. (new) The voltage down converter of claim 1, wherein the trip point is field programmable.

18. (new) The voltage down converter of claim 1, wherein VHYST- and VHYST+ are determined by transistor sizes within the comparator unit.